MS AF
PATENT
8008-1052

IN THE U. S. PATENT AND TRADEMARK OFFICE

In re application of

Yasutaka NAKASHIBA Conf. 2273

Application No. 10/812,282 Group 2815

Filed: March 30, 2004 Examiner Jerome Jackson Jr.

Title: Semiconductor integrated circuit device

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Assistant Commissioner for Patents November 13, 2009
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellant requests a pre-appeal brief review of the final rejection in the above-identified application. No amendments are being filed with this request.

A Notice of Appeal is filed herewith.

The review is requested for the reasons advanced on the attached sheets.

Respectfully submitted,

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REASONS IN SUPPORT OF REQUEST FOR REVIEW

A pre-appeal brief review is respectfully requested because the rejection of the independent claims includes a clear factual error, or in the alternative a legal error, as explained below.

Claims 23-48 are pending. Claims 23 and 36 are the only independent claims and both are the subject of the present request for a pre-appeal brief review.

Claims 23-48 were rejected as unpatentable over KUDO et al. 6,853,037 in view of O 7,088,964 and the admitted prior art (APA).

Claim 23 provides, among other features, that the MOS varactor film (the second insulating film) is thinner than the thinnest of the MOS transistor films (the first insulating films), where the MOS transistor films have a plurality of different thicknesses. Thus, the second insulating film is thinner than all the first insulating films.

The Examiner notes that the claim does not say "all", but claim 23 does state that the second insulating film is thinner than the thinnest of the first insulating films, which is the equivalent of "all." The Examiner also states that "all" is relative and could be defined as the I/O higher threshold transistors. The claim does not include the limitation inserted by the Examiner and the claim should be considered in view of what it actually says - thinner than the thinnest. Adding limitations to the claim is a legal error.

KUDO et al. disclose a semiconductor device with a plurality of MOS transistors having different gate insulating film thicknesses. The film thickness of the n-channel high-voltage transistor is greater than the film thickness of the p-channel high voltage transistor, which is greater than the film thickness of the low-voltage transistor (Abstract). KUDO et al. do not disclose a film thickness of a varactor.

O discloses that "a varactor has an oxide film of which thickness is the same as the MOSFET of the logic device, and has an oxide film thinner than the MOSFET of the I/O device." That is, the film thickness of the I/O transistor is thicker than that of the film thickness of a logic transistor, and the film thickness of the varactor is equal to that of the logic transistor. In O, the gate insulating film of the MOSFET of the logic device corresponds to the "thinnest insulating film among the first insulating films of the MOS transistors" as recited in claim 23.

The APA discloses that "the thickness of the gate insulating film of the MOS type varactor element is the same as the thickness of the gate insulating film of the MOS transistor. The APA also acknowledges that the logic and I/O devices are usually formed on the same chip.

The Examiner notes that the prior art recognizes that varactors are formed from MOS transistor structures and that, therefore, the MOS transistor and varactor could have the same structure. The applicant has taken this into account by

including the limitation at the end of claim 23 that the first and second diffusion layers are provided on both sides of the conductive electrode and that these layers are connected to a common terminal through first and second wiring lines. This limitation avoids the Examiner's interpretation: the two cannot have the same structure. The Examiner's interpretation is a factual error.

Thus, KUDO et al. disclose only the film thicknesses of the transistors, and O discloses that the logic transistor has a film thickness equal to that of the varactor. Combining the references does not suggest to the artisan that the film thicknesses of all the MOS transistors are each to be greater than that of the varactor.

That is, the combination of these three references disclose that in a chip with logic devices and I/O devices, the thinnest gate insulating films among the MOS transistors is to be found in the logic devices. The combination merely discloses that the gate insulating film of the varactors element is the same thickness as that of a gate insulating film of the thinnest MOS transistor on the chip. There is nothing in the combination that discloses that the thickness of the second gate insulating film in the varactor element is thinner than the thinnest gate insulating film among the first gate insulating films of the MOS transistors with different thicknesses.

Claim 36 provides that the MOS transistor films all have a same thickness. Thus, the second insulating film is thinner than all the first insulating films. The references do not disclose this. As explained above, the I/O transistor film thickness is greater than that of the logic film thickness, where the logic film thickness is the same as, not less than, the varactor film thickness.

Accordingly, the rejection of claims 23 and 36 includes a factual error, or in the alternative, a legal error.

The dependent claims are patentable at least for depending from an allowable independent claim.

In view of this, it is believed that the rejection of record include a clear factual and/or legal error and cannot be sustained and must be reversed, and such is respectfully requested.